IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Jerome M. Eldridge et al.	Examiner:	Tu-Tu V. Ho
Serial No.:	10/781,035	Group Art Unit:	2818
Filed:	February 18, 2004	Docket:	1303.063US2
Title:	GRADED COMPOSITION METAL OXIDE TUNNEL BARRIER INTERPOLY INSULATORS		

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicants respectfully request that this Supplemental Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants request that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicants with the next official communication.

Pursuant to 37 C.F.R. §1.97(c)(2), Applicants have included the fee of $180.00 as set forth in 37 C.F.R. §1.17(p). Please charge any additional fees or credit any overpayment to Deposit Account No. 19-0743.

The Examiner is invited to contact the Applicants' Representative at the below-listed telephone number if there are any questions regarding this communication.

The present application is either a U.S. national patent application filed after June 30, 2003 or an international application that entered the national stage under 35 U.S.C. § 371 after June 30, 2003. Thus, Applicant believes that the U.S. Patent & Trademark Office has waived the requirement under 37 C.F.R. 1.98 (a)(2)(i) for submitting a copy of each cited U.S. patent and each U.S. patent application publication. The waiver is provided in a pre-OG notice from the U.S. Patent & Trademark Office entitled "Information Disclosure Statements May Be Filed

Without Copies of U.S. Patents and Published Applications in Patent Applications filed after June 30, 2003" and dated July 11, 2003. Applicant acknowledges the requirement to submit copies of foreign patent documents and non-patent literature in accordance with 37 C.F.R. 1.98(a)(2).

Respectfully submitted,

JEROME M. ELDRIDGE ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6960

Date 9-22-04

By Marvin L. Beekman
Reg. No. 38,377

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 22nd day of September, 2004.

Name Amy Moriarty

Signature

PTO/SB/08A(10-01)
Approved for use through 10/31/2002. OMB 651-0031
US Patent & Trademark Office: U.S. DEPARTMENT OF COMMERCE

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if known

Application Number	10/781,035
Filing Date	February 18, 2004
First Named Inventor	Eldridge, Jerome
Group Art Unit	2818
Examiner Name	Ho, Tu-Tu
Attorney Docket No:	1303.063US2

US PATENT DOCUMENTS

Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	Filing Date If Appropriate
	US20010013621	08/01/2001	Nakazato, Kazuo	257	314	12/08/2000
	US-4,449,205	05/15/1984	Hoffman, Charles R.	365	182	02/19/1982
	US-4,495,219	01/22/1985	Kato, Takashi , et al.	427	82	10/08/1982
	US-4,688,078	08/18/1987	Hseih, Ning	257	321	12/11/1985
	US-4,717,943	01/05/1988	Wolf, Hans P., et al.	357	23.5	07/16/1986
	US-4,794,565	12/27/1988	Wu, Albert T., et al.	365	185	09/15/1986
	US-4,870,470	09/26/1989	Bass Jr., Roy S., et al.	357	23.5	10/16/1987
	US-4,939,559	07/03/1990	DiMaria, D. J., et al.	257	38	04/01/1986
	US-5,445,984	08/29/1995	Gary, Hong , et al.	437	43	11/28/1994
	US-5,455,792	10/03/1995	Yi, Yong-Wan	365	185.12	09/09/1994
	US-5,510,278	04/23/1996	Bich-Yen, Nguyen , et al.	437	40	09/06/1994
	US-5,617,351	04/01/1997	Bertin, Claude L., et al.	365	185.05	06/05/1995
	US-5,646,430	07/08/1997	Kaya, Cetin , et al.	257	322	08/28/1995
	US-6,127,227	10/03/2000	Lin, Chrong J., et al.	438	261	01/25/1999
	US-6,169,306	01/02/2001	Gardner, Mark I., et al.	257	310	07/27/1998
	US-6,288,419	09/11/2001	Prall, Kirk D., et al.	257	213	07/09/1999
	US-6,377,070	04/23/2002	Forbes, Leonard	326	41	02/09/2001
	US-6,514,842	02/04/2003	Prall, K. D., et al.	438	593	08/08/2001
	US-6,730,575	05/04/2004	Eldridge, Jerome M.	257	310	08/30/2001

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T [2]
		HAN, KWANGSEOK , "Characteristics of P-Channel Si Nano-Crystal Memory", IEDM Technical Digest, International Electron Devices Meeting, (December 10-13, 2000),309-312	
		INUMIYA, S , et al., "Conformable formation of high quality ultra-thin amorphous Ta2 O5 gate dielectrics utilizing water assisted deposition (WAD) for sub 50 nm damascene metal gate MOSFETs", IEDM Technical Digest. International Electron Devices Meeting, (December 10-13, 2000),649-652	
		MANCHANDA, L. , "Si-doped aluminates for high temperature metal-gate CMOS: Zr-Al-Si-O, a novel gate dielectric for low power applications", IEDM Technical Digest. International Electron Devices Meeting, (December 10-13, 2000),23-26	
		YAMAGUCHI, TAKESHI , "Band Diagram and Carrier Conduction Mechanism in ZrO2/Zr-silicate/Si MIS Structure Fabricated by Pulsed-laser-ablation Deposition", Electron Devices Meeting, 2000. IEDM Technical Digest. International, (2000),19-22	

EXAMINER **DATE CONSIDERED**

Substitute Disclosure Statement Form (PTO-1449)

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Jerome M. Eldridge et al.	Examiner: Tu-Tu V. Ho
Serial No.:	10/781,035	Group Art Unit: 2818
Filed:	February 18, 2004	Docket: 1303.063US2
Title:	GRADED COMPOSITION METAL OXIDE TUNNEL BARRIER INTERPOLY INSULATORS	

COMMUNICATION CONCERNING RELATED APPLICATION(S)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Applicants would like to bring to the Examiner's attention the following related application(s) in the above-identified patent application:

Serial/Patent No.	Filing Date	Attorney Docket	Title
09/945507	August 30, 2001	1303.014US1	FLASH MEMORY WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS
09/945395 6754108	August 30, 2001	1303.019US1	DRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY INSULATORS
09/943134	August 30, 2001	1303.020US1	PROGRAMMABLE ARRAY LOGIC OR MEMORY DEVICES WITH ASYMMETRICAL TUNNEL BARRIERS
09/945498 6778441	August 30, 2001	1303.024US1	INTEGRATED CIRCUIT MEMORY DEVICE AND METHOD
09/945512	August 30, 2001	1303.027US1	IN SERVICE PROGRAMMABLE LOGIC ARRAYS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS
09/945554	August 30, 2001	1303.028US1	SRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY INSULATORS

09/945500	August 30, 2001	1303.029US1	PROGRAMMABLE MEMORY ADDRESS AND DECODE CIRCUITS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS
10/028001	December 20, 2001	1303.035US1	PROGRAMMABLE ARRAY LOGIC OR MEMORY WITH P-CHANNEL DEVICES AND ASYMMETRICAL TUNNEL BARRIERS
10/081818	February 20, 2002	1303.045US1	ATOMIC LAYER DEPOSITION OF METAL OXIDE AND/OR LOW ASYMMETRICAL TUNNEL BARRIER INTERPOLY INSULATORS
10/177096	June 21, 2002	1303.063US1	GRADED COMPOSITION METAL OXIDE TUNNEL BARRIER INTERPOLY INSULATORS
10/789038	February 27, 2004	1303.024US2	INTEGRATED CIRCUIT MEMORY DEVICE AND METHOD
10/783695	February 20, 2004	1303.019US2	DRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY INSULATORS
10/929916	August 30, 2004	1303.035US2	PROGRAMMABLE ARRAY LOGIC OR MEMORY WITH P-CHANNEL DEVICES AND ASYMMETRICAL TUNNEL BARRIERS
10/788810	February 27, 2004	1303.027US2	IN SERVICE PROGRAMMABLE LOGIC ARRAYS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS
10/819550	April 7, 2004	1303.019US3	DRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY INSULATORS

10/931704	September 1, 2004	1303.014US2	FLASH MEMORY WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS
10/929986	August 30, 2004	1303.045US2	ATOMIC LAYER DEPOSITION OF METAL OXIDE AND/OR LOW ASYMMETRICAL TUNNEL BARRIER INTERPOLY INSULATORS
10/931711	September 1, 2004	1303.029US2	PROGRAMMABLE MEMORY ADDRESS AND DECODE CIRCUITS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS
10/931540	August 31, 2004	1303.020US2	PROGRAMMABLE ARRAY LOGIC OR MEMORY DEVICES WITH ASYMMETRICAL TUNNEL BARRIERS

Respectfully submitted,

JEROME M. ELDRIDGE ET AL.

By Applicants' Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6960

Date 9-22-04 By _____
Marvin L. Beekman
Reg. No. 38,377

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 22nd day of September, 2004.

Name Amy Moriarty

Signature _____